A Switched-Capacitor Multilevel Inverter Using Series-Parallel Conversion With Reduced Components

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***Abstract*—The switched-capacitor multilevel inverters (SC-MLIs) are the popular type of multilevel inverter. This kind of inverter topology uses the on-off states of switches to control the charging and discharging of capacitors to achieve multilevel output. Most SCMLIs make use of an H-bridge structure to change the polarity of the output voltage, which cause the switches to withstand the peak of the output voltage. The H-bridge is replaced by two half-bridges on both sides of the proposed inverters, and the maximum voltage stress (MVS) on switches in half bridge is kept within 2Vdc, as well as in the extended structure. Therefore, the voltage stress of the switches is greatly reduced. In addition, the topology has a modular structure, which makes the expansion and modulation of the topology simple, while achieving a higher voltage gain. Moreover, with the growth of output levels, the MVS of the switches in the topology remains unchanged, which has good practical application scenarios. In this study, the correctness and feasibility of the topology have been verified by experiments.**

***Index Terms*—Modular, multilevel inverter, switched-capacitor, voltage gain.**

I. Introduction

To achieve net-zero carbon emission, distributed renewable energy generation systems have been widely used thanks to its high reliability, less environmental pollution, low economic cost and system flexibility [1], [2]. Fig. 1 shows the distributed renewable energy generation system, inverters are the key link of power conversion and transmission. Multilevel inverters (MLIs) are widely applied in numerous areas, such as electric vehicles (EVs), renewable energy system, and flexible ac transmission systems. Compared with the conventional two-level inverter, MLIs have lots of excellent features like low total harmonic distortion (THD), reduced d*v*/d*t* on switches, lower switching frequency, etc. [3], [4]. Generally, the classic MLIs are divided into neutral-point clamped (NPC) inverter [5], flying capacitor (FC) inverter [6], and cascaded H-bridge (CHB) inverter [7]. However, the limitation of NPC multilevel inverter mainly lies in the imbalance of capacitor voltage, the same issues can be found on FC multilevel inverter which employs numerous capacitors to obtain appropriate output levels. The CHB inverters can output more levels by using multiple H-bridge cells. However, the demand for multiple isolated dc source limits the application range. With the rapid development of power industry, it is of great significance to find a new high-performance multilevel inverter with fewer devices, more output levels, and higher conversion efficiency [8]–[10].

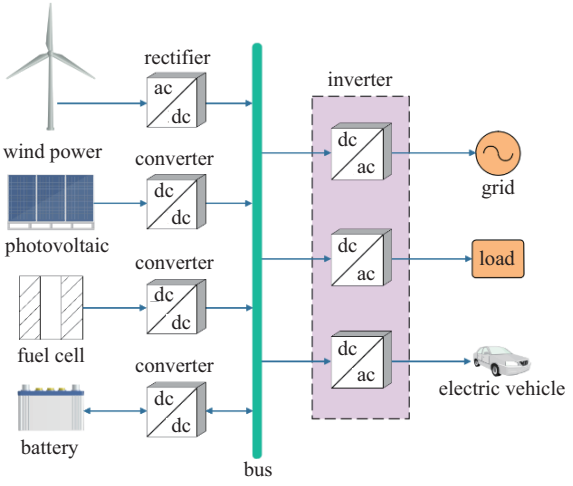

Fig. 1. Distributed renewable energy generation system.

To reduce the number of devices and make the control simpler, the switched capacitor (SC) technology is applied to MLIs in recent years [11]–[14]. SC is a typical non-magnetic structure, which is composed of switching devices and capacitors. SC has the merits of small volume and high-power density. In addition, due to the boosting capability of SC structure, SC inverter can connect the dc input side to the ac output side directly, reducing the need of a too high duty ratio of the intermediate voltage boost link and improving the inverter efficiency. In [15], a single-input switched-

Manuscript received May 1, 2022; revised June 14, 2022; accepted July 29, 2022. Date of publication September 30, 2022; date of current version September 23, 2022. This work was supported in part by the National Natural Science Foundation of China under Grant 51507155, in part by the Youth Key Teacher Project of Henan Universities under Grant 2019GGJS011, and in part by the Key R&D and Promotion Special Project of Henan Province under Grant 222102520001. *(Corresponding author: Wenjun Liu.)*

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Digital Object Identifier 10.24295/CPSSTPEA.2022.00031

capacitor five-level inverter is proposed. The inverter can generate multilevel voltage using a dc source and has the ability of voltage step-up. However, the limited 5-level output produce more voltage harmonics. The 7-level SC topology is presented in [16]. It can reduce the switching device count by the cooperation of series capacitors. However, a complex modulation algorithm is needed to achieve the voltage balance of capacitors. In [17] and [18], some new structures of multilevel converter are presented. These topologies can generate more levels with less switches, but a large number of capacitors and voltage balancing circuits are needed.

In order to output more levels with less devices, some MLIs based on SC with series-parallel conversion are proposed [19]–[21]. In [22], a new cascaded MLI is proposed, which uses symmetric and asymmetric structures to produce even and odd levels. However, a large amount of isolated dc sources is needed with the growth of output levels. In [23], an SCMLI is proposed with voltage boosting capability. This inverter abandons the traditional H-bridge structure, and all power devices just need to withstand the same voltage of dc source. However, numerous devices are employed, which may increase the system cost. In [24], an SCMLI with strong voltage boosting capability and modular expansion capability is proposed, but the strong voltage boosting capability may cause a sharp accumulation of voltage stress on the H-bridge, and increase the total standing voltage (TSV) on switches. The single-phase SC inverter proposed in [25] can generate nine-level using single dc source and cut down the use of switching devices, but two additional modulation algorithms are needed to control the balance of capacitor voltage, which may complicate the control algorithm and increase the number of sensors.

In this article, a novel SCMLI is presented. Through series-parallel conversion between capacitors and dc source, the proposed inverter can generate a lot of output levels with less of power devices. The proposed inverter can be used to drive inductive load independently, and the self-balancing of the capacitor voltage makes it unnecessary for additional voltage equalizing circuits or complex control algorithms. The selective harmonic elimination modulation strategy is used to reduce the switching frequency. Moreover, based on the basic SC unit of the proposed inverter, an extended structure is proposed to further increase output levels.

II. Proposed Multilevel Inverter

A. Circuit Topology

Fig. 2 gives the circuit topology of the presented MLI, which consists of three parts: SC circuit, auxiliary bidirectional switches and polarity conversion circuit. In this topology, V_{dc} is the dc voltage source, which supply energy to capacitors and loads. Switches S_5, S_6, S_7, S_8, S_9 and capacitors C_1, C_2 constitute the SC circuit, which realizes series-parallel conversion between power supply and capacitors, and generates the staircase voltage level. S_{10} and S_{11} are the auxiliary bidirectional switches, which

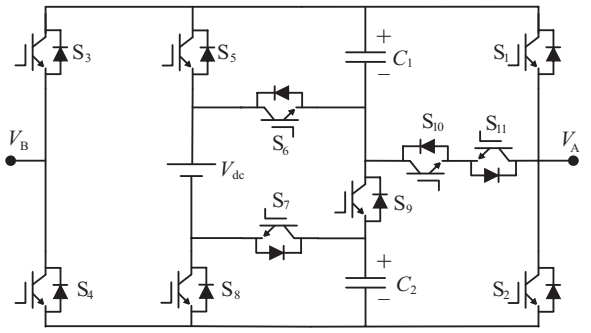

Fig. 2. Circuit topology of the proposed 9-level inverter.

connect the SC circuit and the polarity conversion circuit. S_1, S_2, S_3, S_4 are the switching devices of polarity conversion circuit, which determine the polarity of output voltage. Through the cooperation of the switches, the proposed inverter can output nine levels: $\pm 2V_{dc}$, $\pm 3V_{dc}/2$, $\pm V_{dc}$, $\pm V_{dc}/2$ and 0.

B. State Analysis

Table I lists the operating states of various devices, including on-off states of power switches, and charging and discharging states of capacitor. It can be seen that 1/0 indicate ON/OFF working states of switches, "C", "D", and "–" mean charging, discharging, and idle states of capacitors, respectively. The current paths of the nine-level of the inverter are shown in Fig. 3. Herein, the red solid line represents forward current path, and the blue dotted line represents the reverse current path. To simplify the analysis, assuming that the on-state resistance and forward voltage drop of power switches are zero; the capacitor is large enough and voltage ripple is negligible; the inverter has already entered the steady state.

When the load is a pure resistance load, the working state of the inverter is given in the aforementioned analysis. When the load is inductive, the reverse current paths are marked in blue dotted lines. Each working state of the inverter has a specific path corresponding to the forward current path. Therefore, the proposed topology has the ability to integrate inductive load without additional voltage regulations.

C. Modulation Strategy

To achieve a high-quality of voltage waveform with a low switching frequency, the selective harmonic elimination (SHE) method is used to drive the proposed nine-level topology. By selecting the conducting angle of the switching device, the SHE method can specifically eliminate the target harmonics and decrease the THD of output voltage.

The modulation principle of the SHE is shown in Fig. 4. The nine-level staircase waveform can be seen as the superposition of four quasi-square waveforms V_{oi} ($i = 1, 2, 3, 4$) with the same frequency and amplitude. The amplitude and initial conducting angle of the four quasi-square waveforms are $\pm V_{dc}/2$ and q_i, respectively. These angles satisfy $0 < \theta_1 < \theta_2 < \theta_3 < \theta_4 < \pi/2$.

The Fourier decomposition of each quasi-square waveform V_{oi} can be expressed as

TABLE I
OPERATING STATES OF THE PROPOSED INVERTER

States	Switches											Capacitors		Output levels
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	C_1	C_2	
1	1	0	0	1	0	1	1	0	0	0	0	D	D	$2V_{dc}$
2	1	0	0	1	0	1	0	1	0	0	0	D	–	$3V_{dc}/2$
3	1	0	0	1	0	0	0	0	1	0	0	C	C	V_{dc}
4	0	0	0	1	0	0	0	0	1	1	1	C	D	$V_{dc}/2$
5	0	1	0	1	0	0	0	0	1	0	0	C	C	0
6	0	0	1	0	0	0	0	0	1	1	1	D	C	$-V_{dc}/2$
7	0	1	1	0	0	0	0	0	1	0	0	C	C	$-V_{dc}$
8	0	1	1	0	1	0	1	0	0	0	0	–	D	$-3V_{dc}/2$
9	0	1	1	0	0	1	1	0	0	0	0	D	D	$-2V_{dc}$

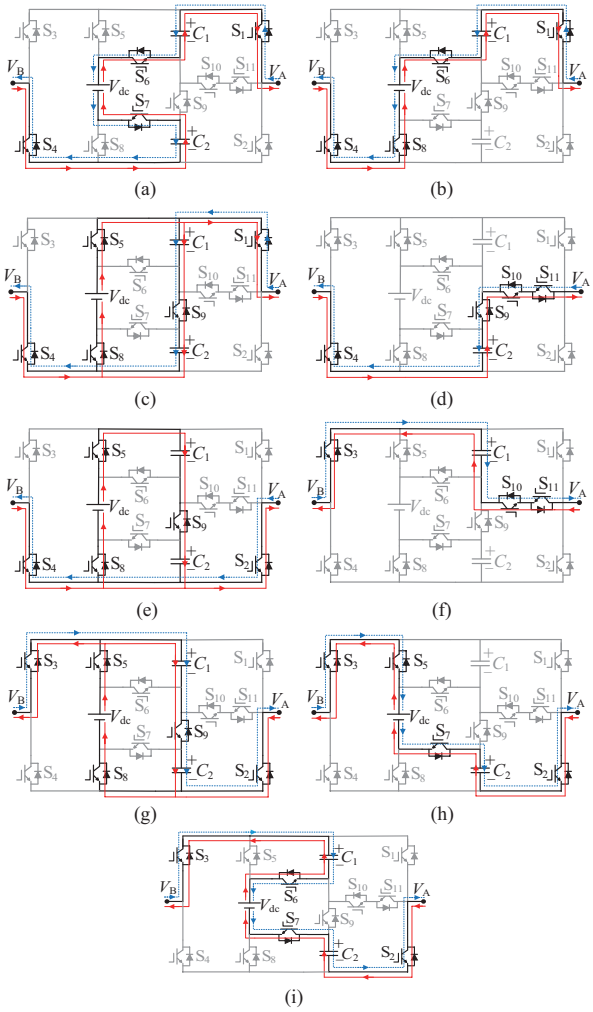

Fig. 3. Current path for proposed inverter. (a) $2V_{dc}$ level, (b) $3V_{dc}/2$ level, (c) V_{dc} level, (d) $V_{dc}/2$ level, (e) zero level, (f) $-V_{dc}/2$ level, (g) $-V_{dc}$ level, (h) $-3V_{dc}/2$ level and (i) $-2V_{dc}$ level.

$$V_{oi} = \frac{2V_{dc}}{\pi} \sum_{k=1,3,\ldots}^{\infty} \frac{\cos(k\theta_i)}{k} \sin(k\omega t) \ , \tag{1}$$

where ω is the angular frequency of the staircase output.

According to the principle of waveform synthesis, the output

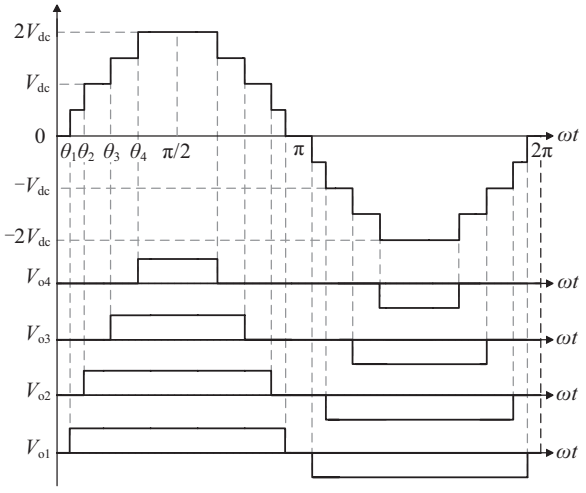

Fig. 4. Modulation principle of the SHE.

voltage can be expressed as

$$V_o = \sum_{i=1}^{4} V_{oi} \ . \tag{2}$$

Thus, the Fourier decomposition of the output voltage V_o is given by

$$V_o = \frac{2V_{dc}}{\pi} \sum_{k=1,3,\ldots}^{\infty} \sum_{i=1}^{4} \frac{\cos(k\theta_i)}{k} \sin(k\omega t) \ . \tag{3}$$

The amplitude modulation index M_{of} is expressed as

$$M_{of} = \frac{1}{4} \sum_{i=1}^{4} \cos\theta_i \ . \tag{4}$$

The THD of the output waveform is given by

$$\mathrm{THD} = \frac{\sqrt{\sum_{k=3,5,\ldots}^{\infty} \left[\sum_{i=1}^{4} \frac{\cos(k\theta_i)}{k} \right]^2}}{\sum_{i=1}^{4} \cos\theta_i} \times 100\% \ . \tag{5}$$

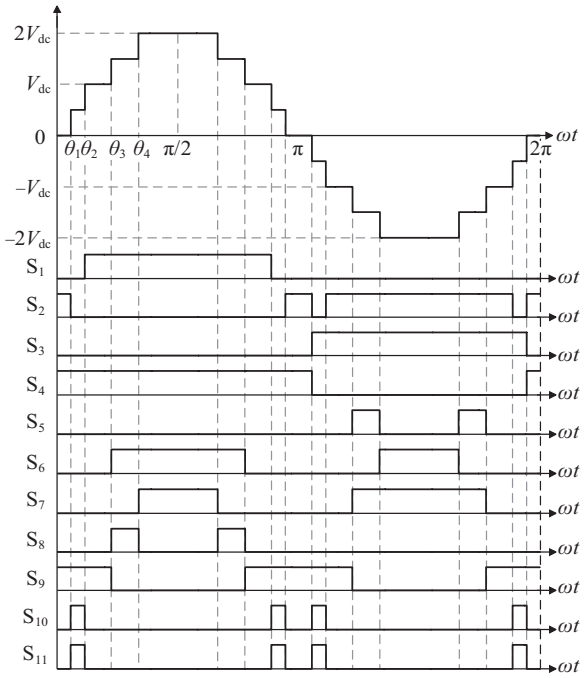

Fig. 5. Operational waveforms of each switching device.

In the output waveforms of the inverter, the low-frequency harmonics are the dominant component of the total harmonic contents. Therefore, selective elimination of low-frequency harmonics can greatly improve the waveform quality of the output voltage. When the 5th, 7th and 11th harmonics are chosen to be removed, the mathematical equations for calculating the conducting angles of each quasi-square waveforms are as follows:

$$\begin{cases} \cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3)+\cos(\theta_4)=4M_{\text{of}} \\ \cos(5\theta_1)+\cos(5\theta_2)+\cos(5\theta_3)+\cos(5\theta_4)=0 \\ \cos(7\theta_1)+\cos(7\theta_2)+\cos(7\theta_3)+\cos(7\theta_4)=0 \\ \cos(11\theta_1)+\cos(11\theta_2)+\cos(11\theta_3)+\cos(11\theta_4)=0 \end{cases} . \quad (6)$$

According to the modulation principle and the operating principle of the proposed inverter, the operating waveforms of the switching devices S_1–S_{11} are shown in Fig. 5. Table II lists the switching frequency and maximum voltage stress (MVS) on power devices. From Table II, the switching frequency is significantly reduced, and the average switching frequency is 2.2 times of the reference frequency. The MVS on switches is twice of the input voltage, and the average voltage stress is 1.2 times of the input voltage. With demonstrated modulation states, the switching frequency and voltage stress are both reduced which can help to cut down the switching losses and prolong the device lifetime.

III. Capacitance Analysis

A. Capacitor Voltage Balance Analysis

For SC inverters, the capacitor voltage balance is crucial to the generation of ideal output voltage. The unbalance of capacitor voltage will lead to output voltage bias, leading to overvoltage, overcurrent, capacitor breakdown etc. which will ultimately lead to system collapse. Therefore, the balance control of capacitor voltage needs special attentions for the stability of inverter system [26], [27]. According to the working principle, the charging circuit of two capacitors does not contain load. Therefore, the charging time and charging current are not affected by the load. In the charging state, the dc source is directly connected with two capacitors to charge them, and the capacitor voltage can reach the rated voltage quickly.

The essence of voltage balance is that the amount of charge and discharge of the capacitor are equal. Fig. 6 gives the charging and discharging status of capacitors and corresponding voltage waveforms in one cycle. It can be seen from the Fig. 6 that the discharging intervals of the capacitor C_1 are $[\theta_3, \pi-\theta_3]$, $[\pi+\theta_1, \pi+\theta_2]$, $[\pi+\theta_4, 2\pi-\theta_4]$ and $[2\pi-\theta_2, 2\pi-\theta_1]$, and the discharging current is the load current i_o.

Therefore, the total discharging amount of the capacitor C_1 in one cycle is

TABLE II
Switching Frequency and MVS on Switches

Switches	Switching frequency	MVS on switches
S_1	f_o	$2V_{dc}$
S_2	$3f_o$	$2V_{dc}$
S_3	f_o	$2V_{dc}$
S_4	f_o	$2V_{dc}$
S_5	$2f_o$	$V_{dc}/2$
S_6	$2f_o$	$V_{dc}/2$
S_7	$2f_o$	$V_{dc}/2$
S_8	$2f_o$	$V_{dc}/2$
S_9	$2f_o$	V_{dc}
S_{10}	$4f_o$	$V_{dc}/2$
S_{11}	$4f_o$	$3V_{dc}/2$

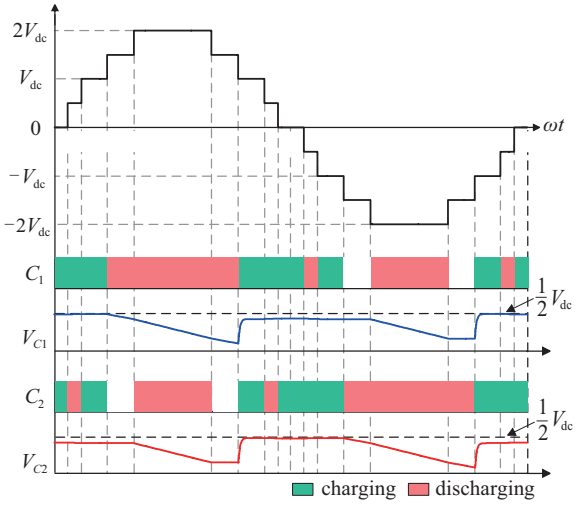

Fig. 6. Operating states of capacitors C_1 and C_2.

$$\Delta Q_1=\frac{1}{2\pi f_o}\left(\int_{\theta_3}^{\pi-\theta_3} i_o\ \mathrm{d}\omega t+\int_{\pi+\theta_1}^{\pi+\theta_2} i_o\ \mathrm{d}\omega t+\int_{\pi+\theta_4}^{2\pi-\theta_4} i_o\ \mathrm{d}\omega t+\int_{2\pi-\theta_2}^{2\pi-\theta_1} i_o\ \mathrm{d}\omega t\right), \tag{7}$$

where f_o is the output frequency, and ω is the angular frequency of the output voltage.

The modulation interval is symmetrical, and the working state of the symmetrical modulation interval is the same. Thus, ΔQ_1 can be calculated by

$$\Delta Q_1=\frac{1}{\pi f_o}\left(\int_{\theta_4}^{\pi-\theta_4}\frac{2V_{dc}}{R_o}\ \mathrm{d}\omega t+\int_{\theta_3}^{\theta_4}\frac{3V_{dc}}{2R_o}\ \mathrm{d}\omega t+\int_{\pi+\theta_1}^{\pi+\theta_2}\frac{V_{dc}}{2R_o}\ \mathrm{d}\omega t\right), \tag{8}$$

where R_o is the load resistance.

From (2), the discharging amount of capacitor C_1 is

$$\Delta Q_1=\frac{V_{dc}}{2\pi f_o R_o}(4\pi-\theta_1+\theta_2-3\theta_3-5\theta_4)\ . \tag{9}$$

The discharging intervals of the capacitor C_2 are $[\theta_1, \theta_2]$, $[\theta_4, \pi-\theta_4]$, $[\pi-\theta_2, \pi-\theta_1]$ and $[\pi+\theta_3, 2\pi-\theta_3]$, and the discharging current is also the load current i_o. Therefore, the total discharging amount of capacitor C_2 in one cycle is

$$\Delta Q_2=\frac{1}{2\pi f_o}\left(\int_{\theta_1}^{\theta_2} i_o\ \mathrm{d}\omega t+\int_{\theta_4}^{\pi-\theta_4} i_o\ \mathrm{d}\omega t+\int_{\pi-\theta_2}^{\pi-\theta_1} i_o\ \mathrm{d}\omega t+\int_{\pi+\theta_3}^{2\pi-\theta_3} i_o\ \mathrm{d}\omega t\right). \tag{10}$$

Further calculation of the above formula:

$$\Delta Q_2=\frac{1}{\pi f_o}\left(\int_{\theta_1}^{\theta_2}\frac{V_{dc}}{2R_o}\ \mathrm{d}\omega t+\int_{\theta_4}^{\pi-\theta_4}\frac{2V_{dc}}{R_o}\ \mathrm{d}\omega t+\int_{\pi+\theta_3}^{\pi+\theta_4}\frac{3V_{dc}}{2R_o}\ \mathrm{d}\omega t\right). \tag{11}$$

Then, the total discharging amount of capacitor C_2 is

$$\Delta Q_2=\frac{V_{dc}}{2\pi f_o R_o}(4\pi-\theta_1+\theta_2-3\theta_3-5\theta_4)\ . \tag{12}$$

From the above calculation results, the total discharging amount of capacitor C_1 is equal to the total discharging amount of capacitor C_2 in one cycle. Therefore, a self-balancing of capacitor voltage can be achieved for the proposed inverter.

B. Capacitor Determination Analysis

Capacitance is usually designed according to the principle that the voltage ripple of capacitor is kept within 10% of the rated capacitor voltage [28], [29]. The voltage ripple is mainly determined by the maximum continuous discharging amount of capacitor. As given in Fig. 6, the maximum continuous discharging interval of C_1 is $[\theta_3, \pi-\theta_3]$. Discharging current is the load current i_o. The maximum continuous discharging interval of capacitor C_2 is $[\pi+\theta_3, 2\pi-\theta_3]$, and the discharging current is still the load current i_o. The maximum continuous discharging interval length and corresponding working status of capacitors C_1 and C_2 are the same. For simple analysis, only capacitor C_1 is calculated. The maximum discharging amount of C_1 is given by

$$\Delta Q=\frac{1}{2\pi f_o}\int_{\theta_3}^{\pi-\theta_3} i_o\,\mathrm{d}\omega t\ . \tag{13}$$

In the interval $[\theta_3, \theta_4]$ and $[\pi-\theta_4, \pi-\theta_3]$, the output voltage is $3V_{dc}/2$. In the interval $[\theta_4, \pi-\theta_4]$, the output voltage of the inverter is $2V_{dc}$. The maximum continuous discharging amount ΔQ can be further calculated by

$$\Delta Q=\frac{1}{2\pi f_o}\left[\int_{\theta_3}^{\theta_4}\frac{3V_{dc}}{2R_o}\mathrm{d}\omega t+\int_{\theta_4}^{\pi-\theta_4}\frac{2V_{dc}}{R_o}\mathrm{d}\omega t+\int_{\pi-\theta_4}^{\pi-\theta_3}\frac{3V_{dc}}{2R_o}\mathrm{d}\omega t\right]. \tag{14}$$

Therefore, the maximum continuous discharging amount is

$$\Delta Q=\frac{V_{dc}(2\pi-3\theta_3-\theta_4)}{2\pi f_o R_o}\ . \tag{15}$$

According to the design principle that the voltage ripple should be kept within 10% of the rated voltage of capacitors. Hence, the capacitance of C_1 and C_2 must satisfy

$$C\geqslant\frac{\Delta Q}{0.1V_c}\ . \tag{16}$$

where V_c is the rated voltage of C_1 and C_2.

Under the condition of allowable voltage ripples, the minimum capacitance is

$$C_{min}=\frac{V_{dc}(2\pi-3\theta_3-\theta_4)}{2\pi f_o R_o\Delta U_{rip}}\ , \tag{17}$$

where ΔU_{rip} is voltage ripple of capacitor, and $\Delta U_{rip}\leqslant 10\%\ V_c$.

Fig. 7 gives the relationship of minimum capacitance versus output frequency and load resistance with 10% voltage ripple. The larger the output frequency and load resistance, the smaller the capacitor required by the inverter. On the other hand, a larger capacitor can reduce voltage ripple. However, in practice, a large capacitance means higher cost and will increase the cost and area cover. Therefore, the capacitance selection is a trade-off between cost and performance.

IV. Analyses of Power Losses

In the study, power losses of the inverters are calculated,

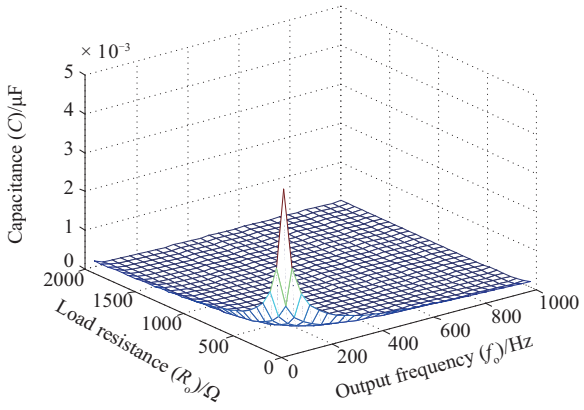

Fig. 7. Relationship of capacitance versus frequency and load resistance.

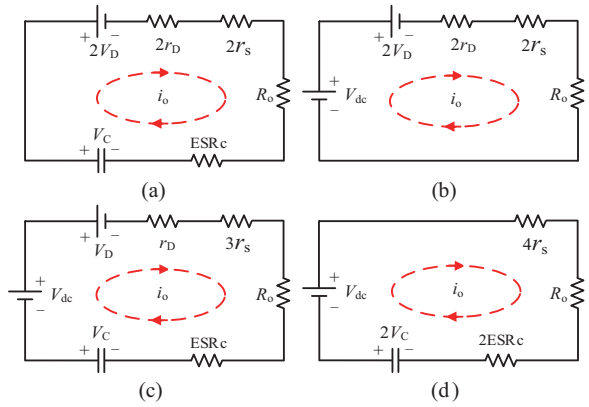

Fig. 8. Equivalent circuits for each working state. (a) States 4, 6, (b) States 3, 7, (c) States 2, 8 and (d) States 1, 9.

which consists of switching losses (P_{sw}), conduction losses (P_{con}) and ripple losses of capacitors (P_{rip}).

A. Conduction Losses

The power losses caused by on-state resistance of power devices and conduction voltage drop of diodes constitute conduction losses. Fig. 8(a)–(d) shows four equivalent circuits corresponding to the nine operating states of the proposed inverters. Assuming that the anti-parallel diodes of switches have the conduction voltage drop V_D and internal resistance r_D; the on-state resistance of switches is r_S and the equivalent series resistance of each capacitor is ESRc.

The equal parameters of four circuits are shown in Table III. Herein, V_{Deq} is the equivalent voltage drop of diode, and r_{eq} is the equivalent resistance of power device.

The total conduction losses are expressed as follows:

$$P_{con}=\frac{2}{\pi}\sum_{i=1}^{4}\left[\left(\frac{V_{out}-V_{Deq}}{r_{eq}+R_o}\right)^2\times r_{eq}\times(\theta_{i+1}-\theta_i)\right]. \tag{18}$$

B. Switching Losses

The switching losses are caused by the turn-on and turn-off processes. According to the linear approximation of the voltage and current, the switching losses of the i-th switch can be calculated as follows:

$$\begin{aligned}P_{sw,on,i}&=f_{sw}\int_0^{t_{on}}v_{sw,i}(t)i(t)\mathrm{d}t\\&=f_{sw}\int_0^{t_{on}}\left(\frac{V_{sw,i}}{t_{on}}t\right)\left[-\frac{I_i}{t_{on}}(t-t_{on})\right]\mathrm{d}t\\&=\frac{f_{sw}V_{sw,i}I_it_{on}}{6},\end{aligned} \tag{19}$$

$$\begin{aligned}P_{sw,off,i}&=f_{sw}\int_0^{t_{off}}v_{sw,i}(t)i(t)\mathrm{d}t\\&=f_{sw}\int_0^{t_{off}}\left(\frac{V_{sw,i}}{t_{off}}t\right)\left[-\frac{I_i}{t_{off}}(t-t_{off})\right]\mathrm{d}t\\&=\frac{f_{sw}V_{sw,i}I_it_{off}}{6},\end{aligned} \tag{20}$$

where f_{sw} is the switching frequency of the i-th switch, $V_{sw,i}$ is the voltage stress on switch, I_i is the current through the i-th switch, t_{on} is the turn-on time and t_{off} is the turn-off time of switch. The total switching losses of proposed inverter is

$$P_{sw}=\sum_{i=1}^{11}\left(P_{sw,on,i}+P_{sw,off,i}\right). \tag{21}$$

According to the aforementioned analysis, the switching frequency and voltage stress of the proposed topology are low, which is helpful to reduce the switching loss of the inverter.

TABLE III
PARAMETERS OF EQUIVALENT CIRCUITS

i	V_{out}	V_{Deq}	r_{eq}
1	$V_{dc}/2$	$2V_D$	$2r_D+2r_S+$ESRc
2	V_{dc}	$2V_D$	$2r_D+2r_S$
3	$3V_{dc}/2$	V_D	r_D+3r_S+ESRc
4	$2V_{dc}$	0	$4r_S+2$ESRc

C. Ripple Losses

The ripple loss is caused by the voltage fluctuation of capacitor. The voltage ripple can be calculated by

$$\Delta U_{rip}=\frac{V_{dc}(2\pi-3\theta_3-\theta_4)}{2\pi f_o R_o C}. \tag{22}$$

The ripple losses of two capacitors can be calculated as

$$P_{rip}=\sum_{k=1}^{2}C_k\Delta U_{rip}^2 f_o\ . \tag{23}$$

Since the total ripple loss of the inverter is

$$P_{rip}=\frac{V_{dc}^2(2\pi-3\theta_3-\theta_4)^2}{2\pi^2 f_o R_o^2 C}. \tag{24}$$

TABLE IV
COMPARISON OF THE PROPOSED INVERTER WITH OTHER NINE-LEVEL SCMLI

Topology	N_{Switch}	N_{Diode}	$N_{Capacitor}$	N_{Source}	TSV	Boosting factor	Self-balancing	Expanding ability	Efficiency	CF
[18]	8	3	4	1	6	1	NO	YES	92.8%	29
[19]	10	4	4	1	8	1	YES	YES	93.5%	36
[20]	8	3	3	1	23	4	YES	NO	93%	45
[23]	19	3	3	1	19	4	YES	YES	88.93%	63
[28]	8	6	3	1	26	4	YES	YES	91.6%	51
Proposed topology	11	0	2	1	13	2	YES	YES	94.8%	36

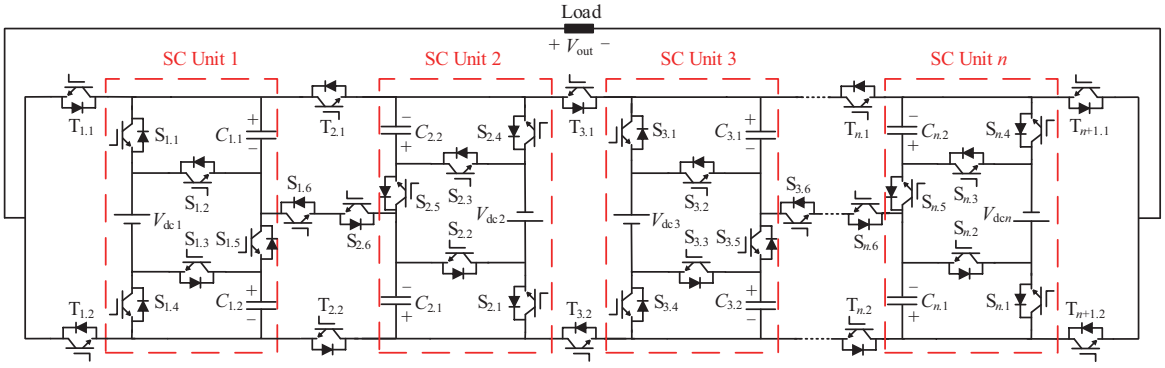

Fig. 9. The proposed extended structure.

The ripple loss is relevant to the operating frequency and capacitance, since a higher operating frequency and larger capacitance can reduce the ripple loss of the inverter. Overall, total power loss of the inverter is summarized as

$$P_{total} = P_{rip} + P_{con} + P_{switch} . \tag{25}$$

The efficiency of the topology is given by

$$\eta = \frac{P_{out}}{P_{rip} + P_{con} + P_{switch} + P_{out}} , \tag{26}$$

where P_{out} is the output power.

V. COMPARISON AND DISCUSSION

In order to appraise the proposed inverter comprehensively, the comparison with the recently proposed SCMLIs has been carried out, as shown in Table IV. The total proposed inverter employs lowest components to output 9-level. Moreover, the proposed topology has the advantages of voltage gain, structure expanding, capacitor voltage self-balancing, and can be used to drive inductive load.

The comparative results of Table IV indicate that both inverters proposed in [18] and [19] have the minimum TSV but they lack the ability to boost voltage. The least switches are employed in the SCMLI of [20]. However, more diodes and capacitors are used. The inverter proposed in [23] has the largest number of switches, which leads to the increase of cost function (CF). Although the boosting factor is 4, the inverter proposed in [28] employs more devices and the TSV is highest.

The proposed topology can output nine-level with only two capacitors. In addition, the voltage gain of 2 can be achieve and the TSV is reduced. Moreover, the proposed inverter has better performance in CF and a higher efficiency due to the use of selective harmonic elimination modulation strategy. The CF is expressed as

$$\mathrm{CF} = (N_{drive} + N_{switch} + N_{diode} + N_{capacitor} + \alpha \mathrm{TSV})\, N_{source} , \tag{27}$$

in which N_{drive} is the number of driver gate, and the number of dc source is N_{source}.

The factor α is used to indicate the significance of TSV, and it is set to 1.0 here. The CF of the inverter is compared in Table IV. It seemed obvious from the table that the CF of the proposed inverter is lower, which is due to its less devices and lower voltage stress.

Based on the aforementioned comparison, the proposed topology has the merits of single input source, low power device count, self-balancing of capacitor voltage, expansion ability, and feasibility of inductive loads. These advantages are helpful to expand the application range of the inverter.

VI. EXTENDED STRUCTURE OF THE PROPOSED INVERTER

The single SC unit in [24] and [30] can output more levels

by cascading. To generate larger number of output levels, the proposed nine-level topology can be extended with multiple SC units, as shown in Fig. 9. The extended structure of the proposed topology is replenished by several SC units, which are connected by polarity conversion switches and auxiliary bidirectional switches.

In the proposed extended structure, the dc source of each SC unit is connected in parallel with its related capacitors, and the capacitor can be charged to $0.5V_{dc}$. Thereby, the output levels are improved by adding SC units. The number of dc sources, capacitors, and power switches for proposed extended structure is expressed as follows:

$$N_{source} = n \,, \tag{28}$$

$$N_{capacitor} = 2n \,, \tag{29}$$

$$N_{switch} = 8n + 1 \,. \tag{30}$$

For the same circuit configuration, the proposed extended structure can work under symmetrical and asymmetrical dc sources.

A. Symmetric Case

In symmetric case, the voltage of all dc sources is equal. The total number of output levels for the proposed extended structure can be obtained as follows:

$$N_{level,\,sym} = 8n + 1 \,. \tag{31}$$

The maximum output voltage of the extended structure is equal to

$$V_{o,\,max,\,sym} = 2nV_{dc} \,, \tag{32}$$

where the voltage of all dc sources is equal to V_{dc}.

B. Asymmetric Case

In asymmetric case, in order to obtain the maximum number of output levels, the value of dc voltage sources should meet the following requirements:

$$V_{dc\,i} = (5)^{i-1} V_{dc} \quad i = 2,...,n. \tag{33}$$

The output levels and the maximum output voltage of the extended structure in asymmetric case is equal to

$$N_{level,\,asym} = 2 \times 5^n - 1 \,, \quad n \geqslant 2 \,, \tag{34}$$

$$V_{o,\,max,\,asym} = \frac{1}{2}(5^n - 1)V_{dc} \,, \quad n \geqslant 2 \,. \tag{35}$$

The proposed extended structure is extended from the proposed nine-level inverter, so the characteristics of the extended structure are the same with the proposed nine-level inverter.

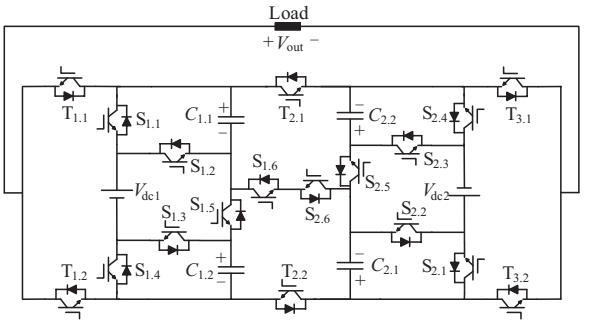

Fig. 10. The topology of double SC units.

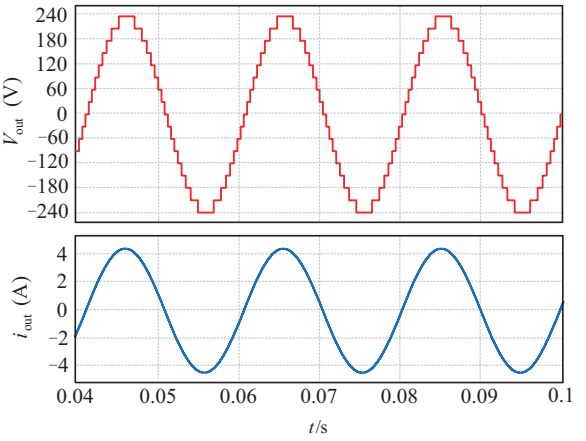

Fig. 11. The simulation results of extended structure.

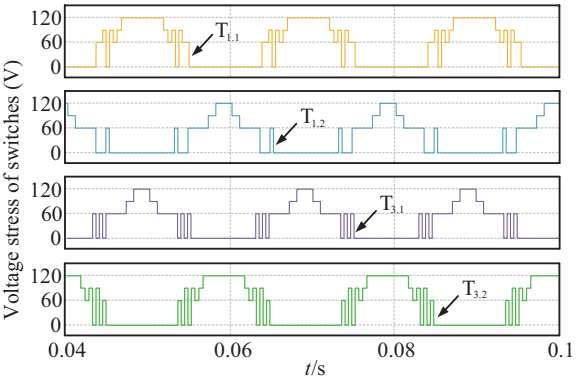

Fig. 12. The voltage stress of switches.

Fig. 10 presents the topology of double SC units. When the both dc sources are 60 V, the simulation results with resistive-inductive load (50 Ω-10 mH) are shown in Fig. 11. It can be seen that the extended structure can generate 17-level by employing double SC units. Moreover, the voltage stress of switches $T_{1.1}$, $T_{1.2}$, $T_{3.1}$ and $T_{3.2}$ are shown in Fig. 12. With the increase of output levels, the MVS of switches in two half bridges can be kept within $2V_{dc}$.

VII. Experimental Results

To verify the correctness and feasibility of the proposed

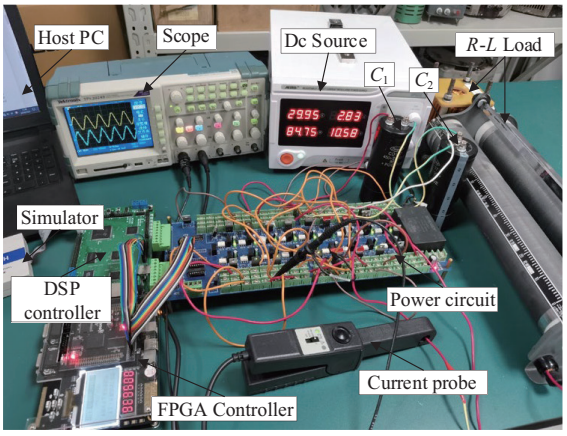

Fig. 13. Experimental Prototype.

TABLE V
EXPERIMENTAL PARAMETERS

Parameters	Value
Dc voltage source (V_{dc})	190 V
Capacitor (C_1, C_2)	2200 μF
Resistance load (R)	100 Ω
Resistive-inductive load (R-L)	50 Ω-10 mH
Reference frequency (f_o)	50 Hz

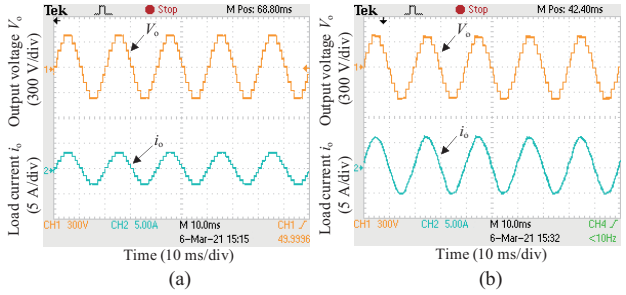

Fig. 14. Experimental results. (a) Output voltage and load current under R load. (b) Output voltage and load current under R-L load.

inverter, an experimental prototype was built as shown in Fig. 13. The experimental parameters are listed in Table V.

A. Steady-State Experimental Results and Analysis

To validate the feasibility of proposed topology and the correctness of its theoretical analysis, the steady-state experiments are conducted.

Fig. 14(a) gives the experimental results of the output voltages and load current when the load is purely resistive. It's obvious that the output voltage and current are ideal nine-level staircase waveforms, which confirms the correctness of the proposed topology and the feasibility of the modulation scheme. Fig. 14(b) gives the experimental waveforms of output voltages and load current when the load is resistive-inductive. It can be seen that output voltage is standard nine-level staircase waveform, and the load current is smoothed and close to the sine waveform. This experimental result proves that the proposed topology can integrate inductive loads.

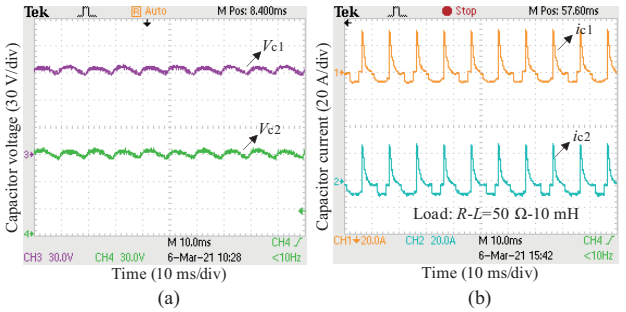

Fig. 15. The experimental results of capacitors. (a) Waveforms of capacitor voltage. (b) Waveforms of capacitor current with R-L load.

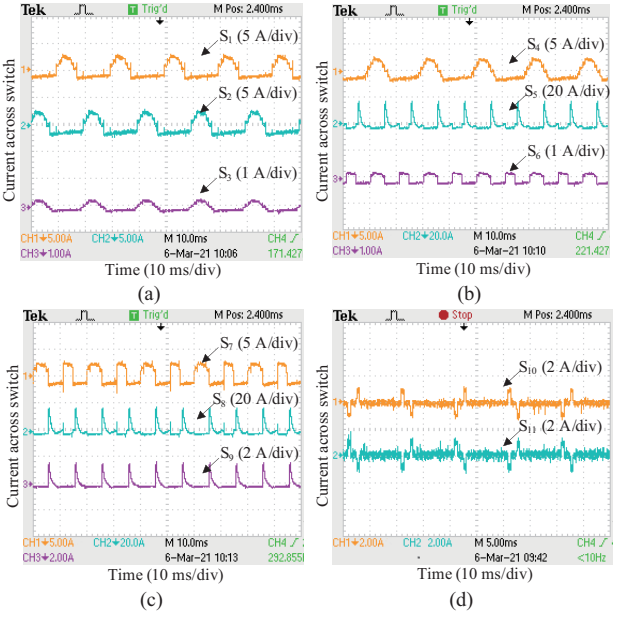

Fig. 16. Experimental results of the current across each switch. (a) Current across switches S_1, S_2, and S_3. (b) Current across switches S_4, S_5, and S_6. (c) Current across switches S_7, S_8, and S_9. (d) Current across switches S_{10} and S_{11}.

Fig. 15 gives the voltage waveforms of two capacitors. As shown in Fig. 15(a), when the system enters steady state, the voltage of two capacitors is stable around the rated voltage, which verifies the self-balancing characters of capacitor voltage. Fig. 15(b) shows the current waveforms of two capacitors under resistive inductive load.

Fig. 16 shows the current stress of each power switch. The results of the proposed inverter are in good agreement with theoretical analysis.

The driving signals for all switches are given in Fig. 17. The switching frequency is significantly reduced by using SHE modulation strategy.

Fig. 18 shows the THD results based on fast Fourier transformation (FFT). It seemed obvious that the THD of output voltage and load current are 9.92% and 1.40%, respectively. The effect of inductive load is similar to filter,

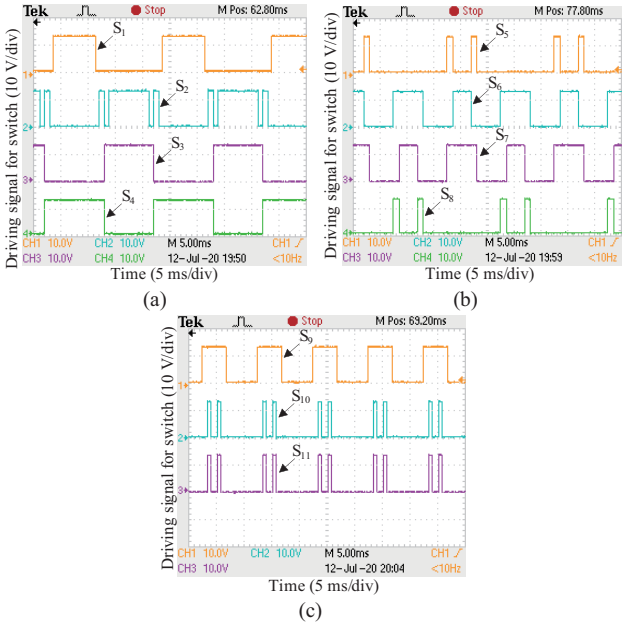

Fig. 17. Experimental waveforms of driving signals. (a) Driving signals for switches S_1, S_2, S_3, and S_4. (b) Driving signals for switches S_5, S_6, S_7, and S_8. (c) Driving signals for switches S_9, S_{10} and S_{11}.

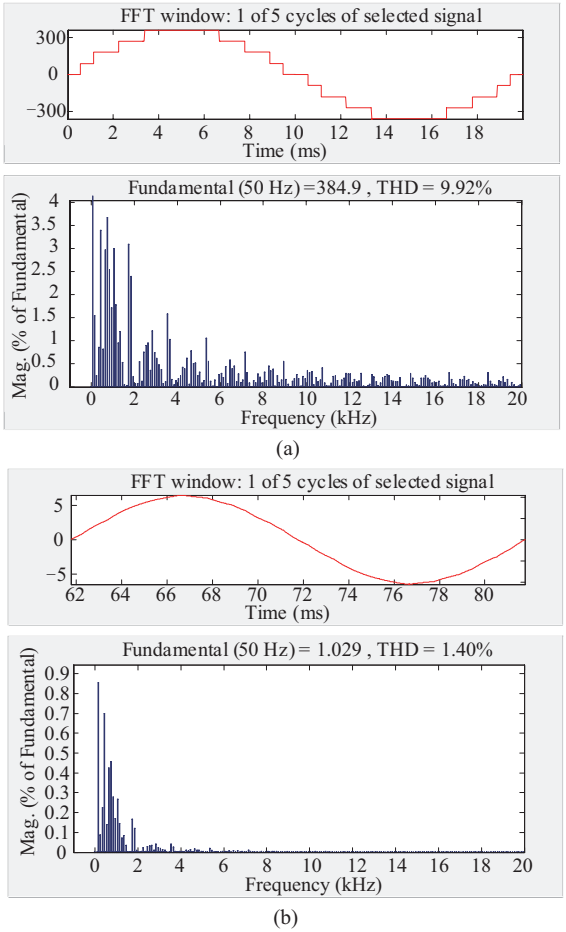

Fig. 18. THD of the output waveforms. (a) The harmonic spectrum of output voltage and (b) the harmonic spectrum of load current.

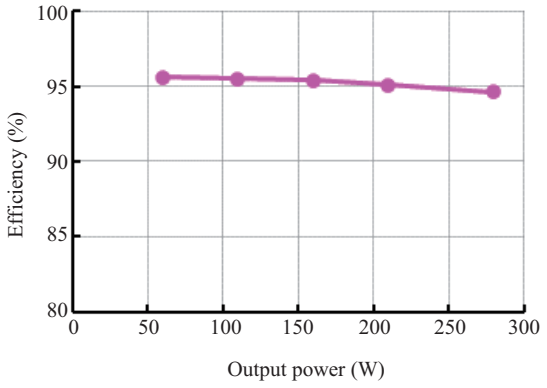

Fig. 19. Efficiencies of the proposed inverter under different powers.

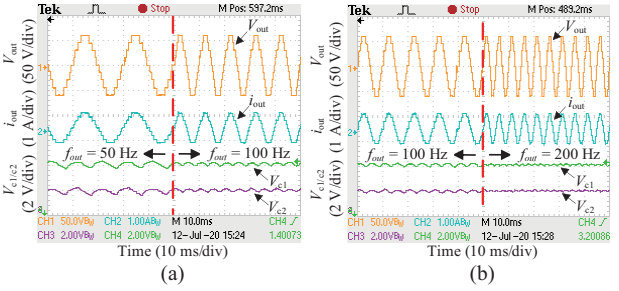

Fig. 20. Dynamic experimental waveforms. (a) f_{out} varies from 50 Hz to 100 Hz. (b) f_{out} varies from 100 Hz to 200 Hz.

and the load current waveform is a smooth sine wave. The proposed inverter has low THD, which verifies the good structure and excellent modulation strategy of the inverter.

The efficiency curve of the proposed inverter is shown in Fig. 19. The important reasons for the high efficiency of the topology are the small number of components and the reduced voltage stress. Moreover, SHEPWM is adopted to greatly reduce the switching frequency. All these factors contribute to improving the efficiency of the inverter.

B. Dynamic Experimental Results and Analysis

To verify the dynamic performance and capacitance self-balancing ability of proposed inverter, several dynamic experiments are conducted, including variable output frequency, loads and input voltage.

Fig. 20 shows the dynamic experimental waveforms of the output voltage, load current and capacitor voltage under variable output frequency f_{out}. In Fig. 20(a), the output frequency varies from 50 Hz to 100 Hz; in Fig. 20(b), the output frequency varies from 100 Hz to 200 Hz. As can be seen from Fig. 20(a) and (b), after the reference frequency changes, the system can enter steady state rapidly. The frequency of output voltage and load current changes to the target frequency, and the capacitor voltage remains stable. The experimental results show that the proposed topology can work in different frequencies.

Fig. 21 shows the dynamic experimental waveforms under variable loads. When the load varies from 0 to resistive load, as shown in Fig. 21(a), the current changes from 0 to nine-level

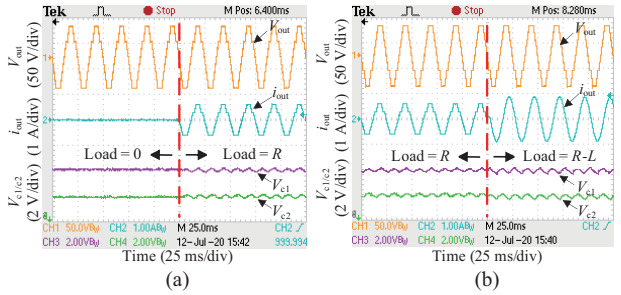

Fig. 21. Dynamic experimental waveforms under variable loads. (a) Load varies from 0 to *R* load. (b) Load varies from *R* to *R-L* load.

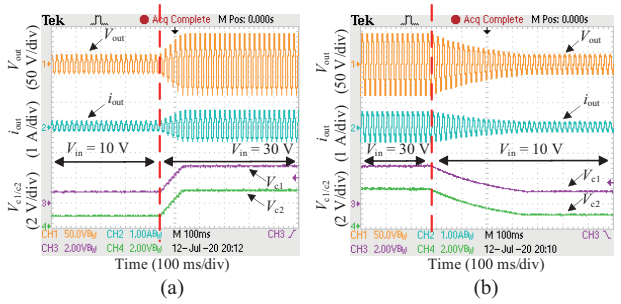

Fig. 22. Dynamic experimental waveforms under variable input voltage. (a) V_{dc} varies from 10 V to 30 V. (b) V_{dc} varies from 30 V to 10 V.

staircase waveform. When the load varies from *R* to *R-L* load, as shown in Fig. 21(b), the output current varies from a nine-level staircase waveform to a smoothed sinusoidal waveform. The experimental results confirm that proposed inverter has excellent robustness and capacitor voltage self-balancing capability.

Fig. 22(a) and (b) shows the dynamic experimental waveforms when input voltage varies from 10 V to 30 V and from 30 V to 10 V, respectively. In Fig. 22(a), when the input voltage changes from 10 V to 30 V, the amplitude of the output voltage increases from 20 V to 60 V and the voltage of capacitors C_1 and C_2 rises synchronously from 5 V to 15 V. In Fig. 22(b), the amplitude of the output voltage decreases from 60 V to 20 V and the voltage of capacitors C_1 and C_2 drops synchronously from 15 V to 5 V when the input voltage varies from 30 V to 10 V. The above experimental results further prove that the proposed inverter has good capacitor voltage self-balancing capability.

VIII. Conclusion

In this study, a novel SCMLI with less devices is presented. Through the series-parallel conversion of SC structure, the proposed topology can output more levels by employing fewer components. The self-balancing of capacitor voltage can be obtained without any auxiliary circuits, and the control strategy is also simplified. The SHEPWM strategy is used to reduce the switching frequency and improve efficiency. Moreover, in order to produce more voltage levels, an extended structure of the proposed topology is proposed with multiple SC units. Symmetric and asymmetry cases for selecting the dc source values have been analysed. Finally, the practicability and correctness of the 9-level topology are verified through steady-state and dynamic experiments. The experimental results indicate that the presented topology has good performance.

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